REMARKS

Initialed Form PTO-1449 Not Provided to Applicant

Applicant submitted along with the initial filing of the present application on February 26, 2004 a Substitute Form PTO-1449 bringing certain references to the attention of the Examiner.

The MPEP states:

> The examiner must consider all citations submitted in conformance with the rules and this section, and their initials when placed adjacent to the considered citations on the list or in the boxes provides a clear record of which citations have been considered by the Office.... If any of the citations are considered, a copy of the submitted list, form PTO-1449, or PTO/SB/08A and 08B, as reviewed by the examiner, will be returned to the applicant with the next communication.
> MPEP 609 III C(2)

Applicant did not receive an initialed copy of this form with the Office Action mailed May 27, 2004.

Applicant respectfully requests that a copy of the initialed form be provided to Applicant. The copy can be included with the next communication from the Patent Office regarding the present application, or can be sent to Applicant's agent via facsimile at the following number: 408-377-6137.

Summary of Claim Status

Claims 1-4 are pending in the present application after entry of the present amendment. Claims 1-4 are rejected for the reasons discussed below.

Applicant requests the favorable reconsideration of the claims and withdrawal of the pending rejections in light of the following remarks.

Rejections Under 35 USC 112

Claims 1-4 are rejected as being indefinite under 35 USC 112, second paragraph. With regard to Claim 1, the Office Action states:

> Claim 1 claims a memory cell formed of complementary NMOS and PMOS transistors comprising a first inverter and a second inverter, etc..., of figure 6 as indicated by applicant. In lines 6-8 and 12-14, it is claimed that the first NMOS and PMOS transistors having respective first gates which provide respective first input nodes of the first inverter, and similarly, the second NMOS and PMOS transistors having respective second gates which provide respective second input nodes of the second inverter. These claimed features are considered unclear for the following reasons.
>
> i) These inverters are claimed to have more than one input node, while they have only one output node.

Applicant respectfully traverses this rejection. In fact, Applicant is confused by the rejection, and is not sure to what the Examiner is objecting. Applying the memory cell of Claim 1 to the circuits of Figs. 6 and 6A, for example, the first and second inverters cited in Claim 1 can be, for example, inverters 161 and 162. Each of inverters 161 and 162 has more than one input node (i.e., two input nodes) and one output node. Therefore, the claim correctly describes the circuits of the figures.

Applicant acknowledges that conventional inverters have only one input node and one output node. However, the memory cells illustrated in Figs. 6 and 6A do not utilize conventional inverters. Further, the term "inverter" is used consistently in the specification to describe circuits 161 and 162, and this usage would be readily understood by those of skill in the art. Applicant respectfully refers the Examiner to MPEP 2173.05(b), which states: "Acceptability of the claim language depends on whether one of ordinary skill in the art would understand what is claimed, in light of the specification."

Therefore, the rejection is not understood. Clarification is requested.

The Office Action further states:

> ii) A node is used in electronic circuit[s] to indicate a terminal, a definite physical point where an electrical contact can be made. Here, with what are claimed as the inverters' input nodes, one could not know, hypothetically, where to put a test probe to observe electrical waves of the inverters' inputs, as these inverters are claimed to have more than one input node.

Applicant respectfully traverses the limiting definition of the term "node" as being equivalent to "a terminal, a definite physical point where an electrical contact can be made", as alleged in the Office Action. The term "node" commonly has a broader interpretation, meaning a common electrical interconnection between one or more physical or virtual elements, and therefore sharing a common voltage level. For example, circuit netlists (e.g., simulation netlists) commonly include many nodes, and a netlist is merely a computer file describing circuit elements and the interconnections between the elements. Therefore, circuit nodes in a netlist certainly are not "definite physical point[s] where an electrical contact can be made", yet they are certainly nodes.

The term "node" can be used to reference a terminal, as stated in the Office Action. However, the term "node" can also refer to, for example, an internal node of a circuit, to which electrical contact may or may not be made (e.g., as the gate nodes of the transistors making up inverters 161 and 162 of Figs. 6 and 6A).

As would be clear to one of skill in the art, two test probes would be required to observe the two input signals for each inverter. One test probe would be placed on each of the two gate nodes of the inverter.

Applicant respectfully requests clarification as to why the Examiner believes it is incorrect to refer to the referenced circuit nodes as "nodes" in Claim 1.

The Office Action further states:

> iii) According to the design, the gates of these first NMOS and PMOS [*sic*, transistors] are intended to be input with coherent electric potentials, supplied by transistors 163 and 164; and similarly for the second inverter's NMOS and PMOS [*sic*, transistors]. According to the figure, if either of [*sic*, or] both of the transistors 163 and 164 malfunction, these inverters' input gates would not receive the intended input potentials, or they may receive voltages that are out of phase. As a result, these inverters' gates no longer serve as the inverters' input nodes as claimed because they depend on other components, which could alter their intended inputs (take for example, voltages from nodes 191 and 192).

Again, Applicant is confused by this explanation of the rejection. If the fact that some event could disrupt an input signal to an input node rendered that input node no longer an input node, no circuit anywhere would have any input nodes at all. Every input signal can be disrupted, yet most circuits have input nodes. Clarification is requested.

Applicant respectfully submits that the terminology used in Claim 1 is fully consistent with the specification. Further, the terminology used in Claim 1 would be readily understood by those of skill in the art, with or without reference to the present specification.

Applicant respectfully draws the Examiner's attention to section 2173.01 of the MPEP, which states:

> A fundamental principle contained in 35 U.S.C. 112, second paragraph is that applicants are their own lexicographers. They can define in the claims what they regard as their invention essentially in whatever terms they choose so long as the terms are not used in ways that are contrary to accepted meanings in the art.... As noted by the court in *In re Swinehart*, 439 F.2d 210, 160 USPQ 226 (CCPA 1971), a claim may not be rejected solely because of the type of language used to define the subject matter for which patent protection is sought.

Therefore, Applicant respectfully requests reconsideration and withdrawal of the rejection of Claim 1.

Claims 2-4 are apparently rejected as indefinite due to their dependency from a rejected base claim, Claim 1. Therefore, Claims 2-4 are also believed allowable over the 35 USC 112 rejection.

Applicant respectfully acknowledges the Examiner's statement that Claim 1 is in potential condition for allowance other than the rejection under 35 USC 112 addressed above. Therefore, all claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested. If any action other than allowance is contemplated by the Examiner, the Examiner is respectfully requested to telephone Applicant's agent, Lois D. Cartier, at 720-652-3733.

Respectfully submitted,

Lois D. Cartier
Agent for Applicant
Reg. No. 40,941

I hereby certify that this correspondence is being deposited with the United States Postal Service as **first class mail** in an envelope addressed to: Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450, on June 22, 2004.

Pat Slaback
Name

Signature